

FIG. 1

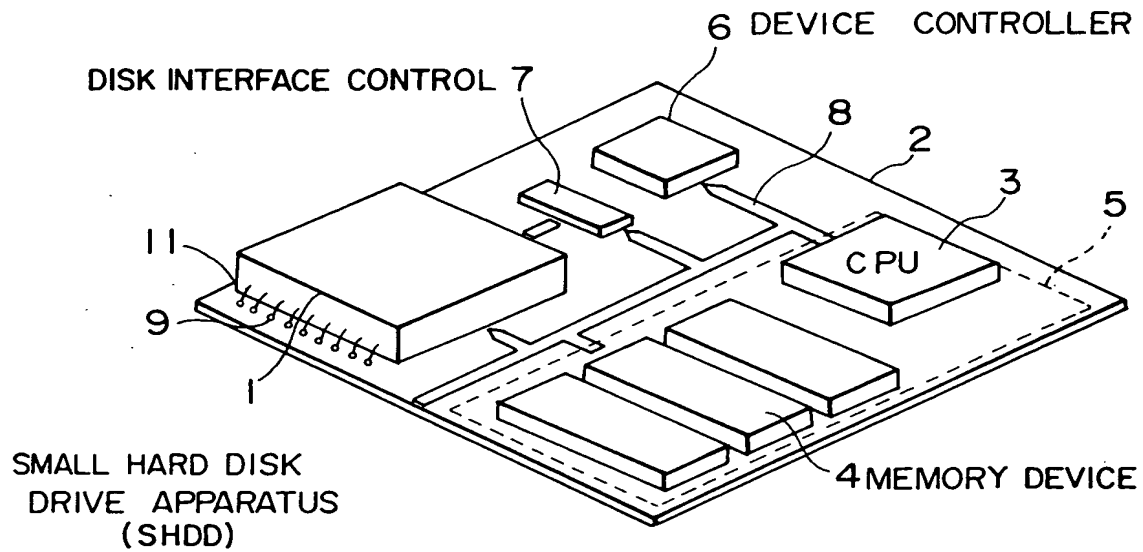
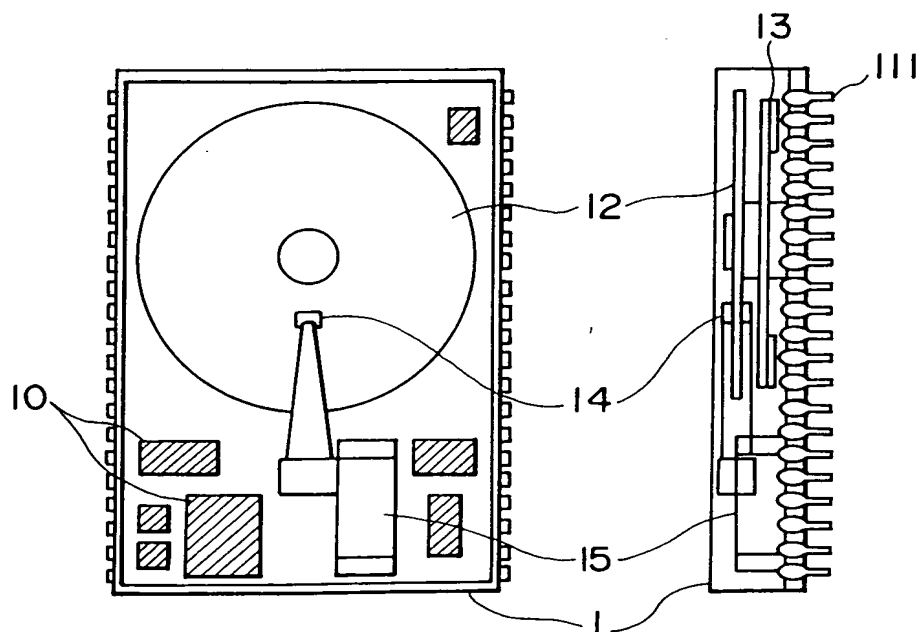


FIG. 2



00015502 022101
10T220 2252T060

FIG. 3

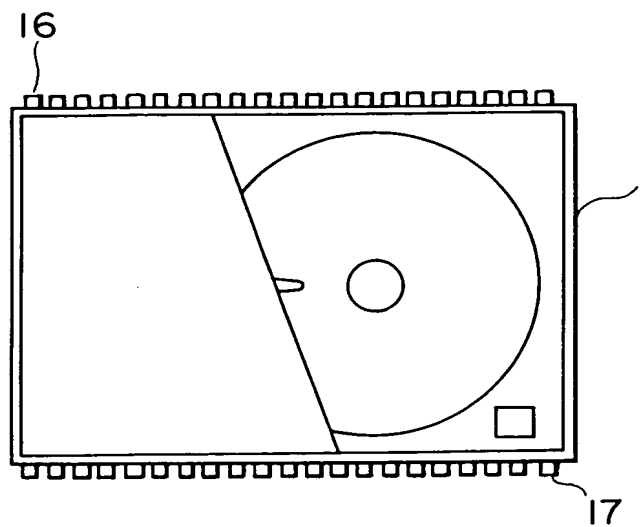
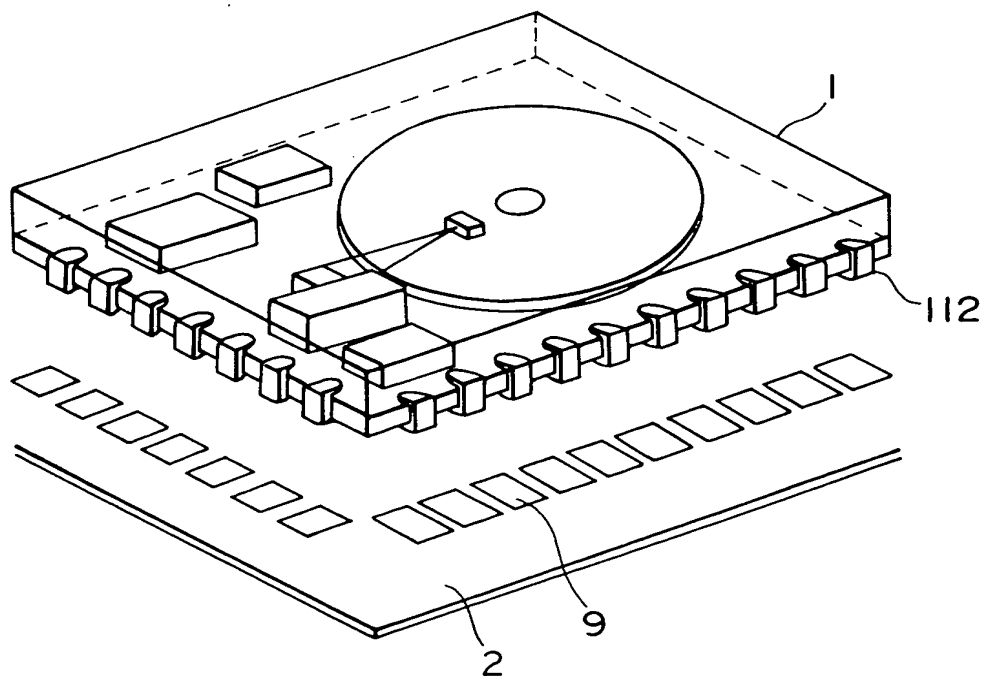


FIG. 4



FOOTED 22521560

FIG. 5

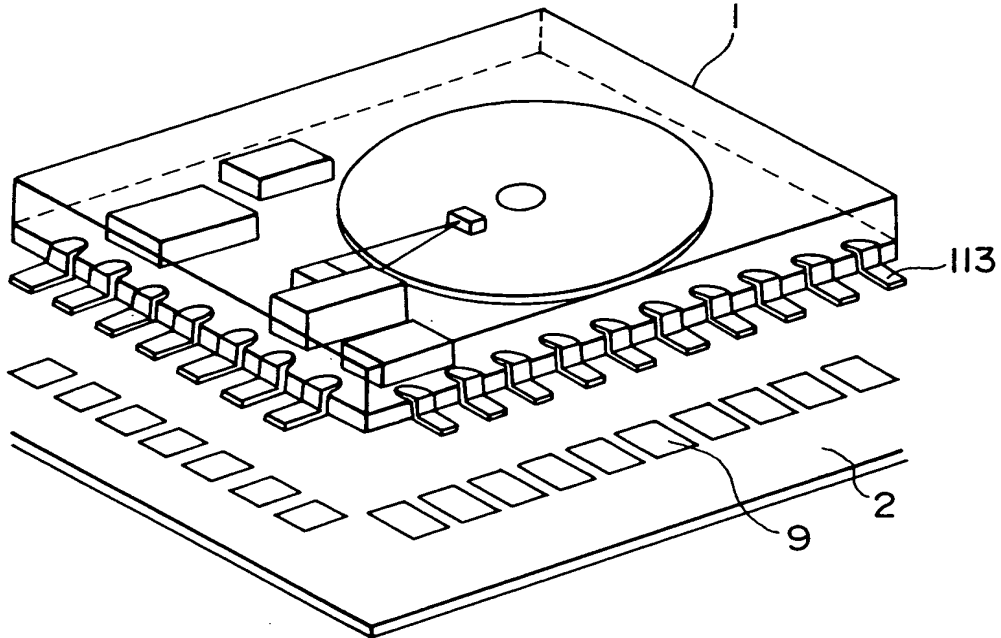


FIG. 6

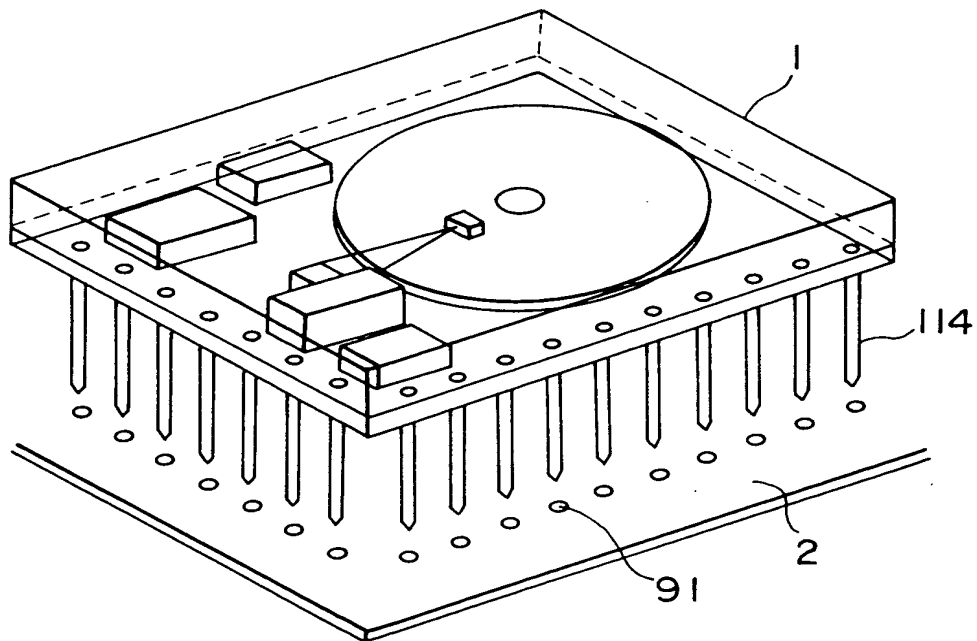


FIG. 7

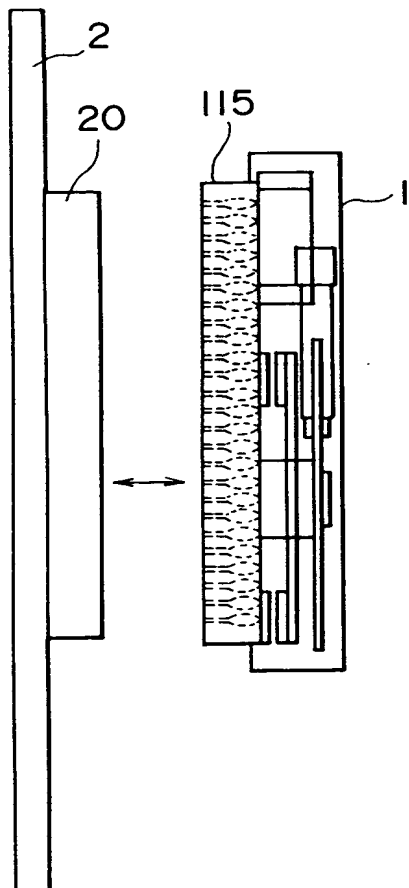


FIG. 8

PIN NO	SIGNAL NAME	PIN NO	SIGNAL NAME
01	GND	02	DB 0
03	GND	04	DB 1
05	GND	06	DB 2
07	GND	08	DB 3
09	GND	10	DB 4
11	GND	12	DB 5
13	GND	14	DB 6
15	GND	16	DB 7
17	GND	18	DB P
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	OPEN	26	TERM PWR
27	GND	28	GND
29	GND	30	GND
31	GND	32	ATN
33	GND	34	GND
35	GND	36	BSY
37	GND	38	ACK
39	GND	40	RST
41	GND	42	MSG
43	GND	44	SEL
45	GND	46	C / D
47	GND	48	REQ
49	GND	50	I / O

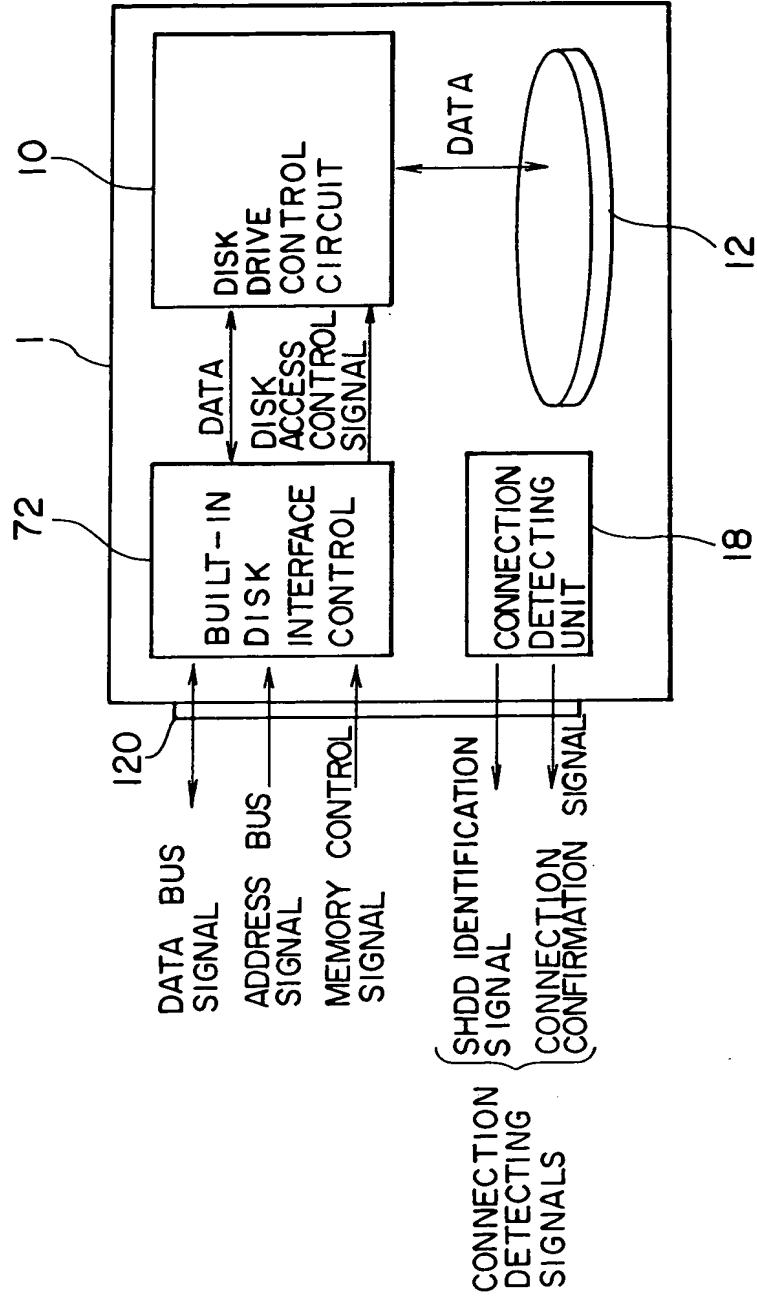
FIG. 9

PIN NO	SIGNAL NAME	PIN NO	SIGNAL NAME
01	ATN	02	DB 0
03	BSY	04	DB 1
05	ACK	06	DB 2
07	RST	08	DB 3
09	MSG	10	DB 4
11	SEL	12	DB 5
13	C / D	14	DB 6
15	REQ	16	DB 7
17	I / O	18	DB P

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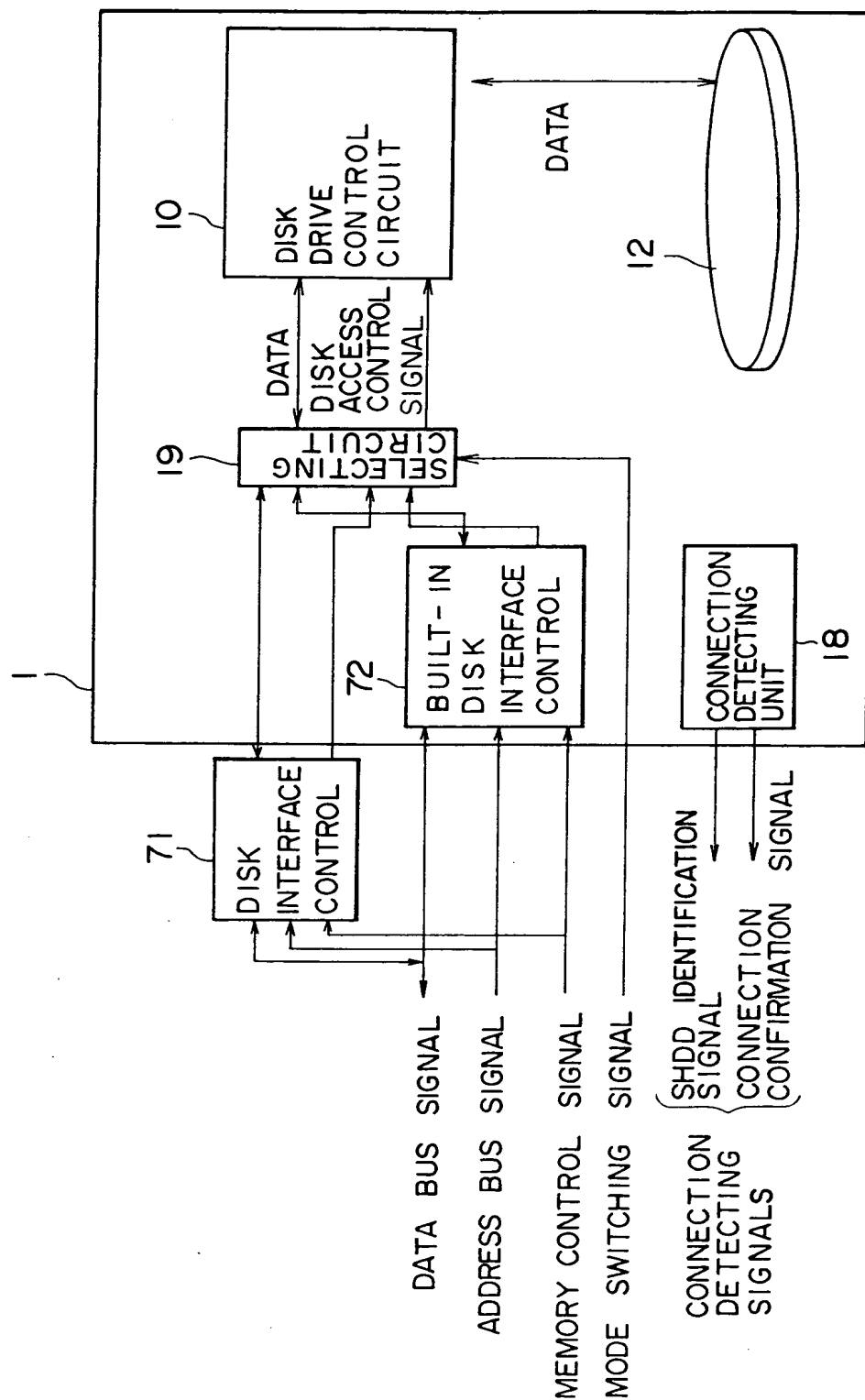
APPROVED	C. C. FIG	
BY	DATE	SUBCLASS
DRAFTSMAN		

FIG. 10



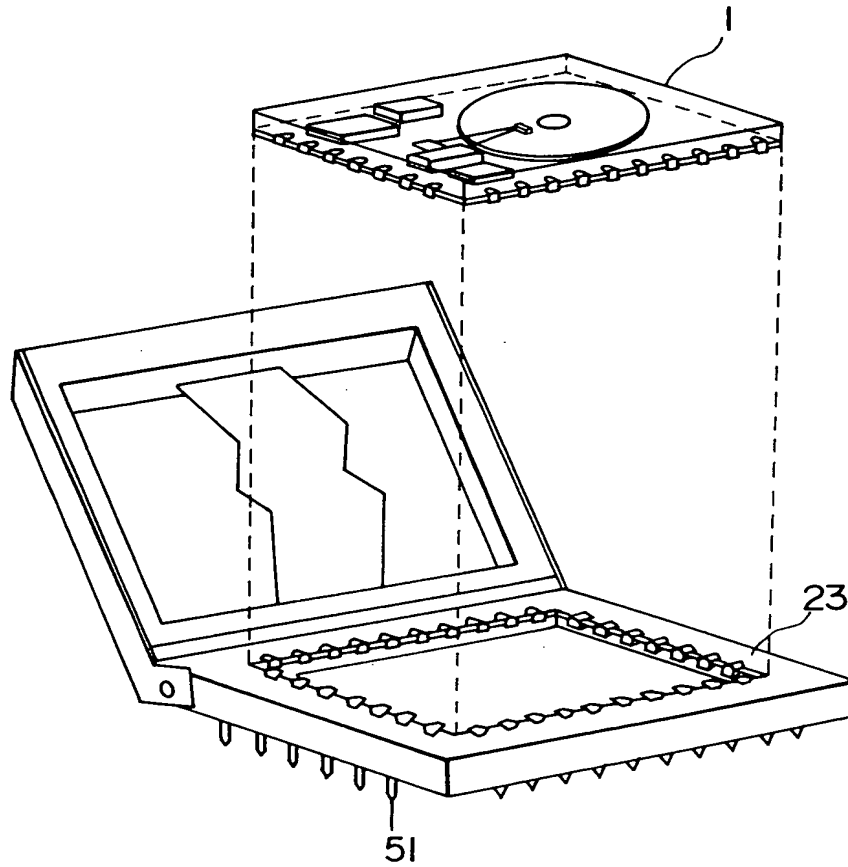
APPROVED	C. S. FIG
av	CLASS
DRAFTSMAN	CLASS

FIG. 13



APPROVED	C. C. FIG	
BY	CLASS	SUBCLASS
DRAFTSMAN		

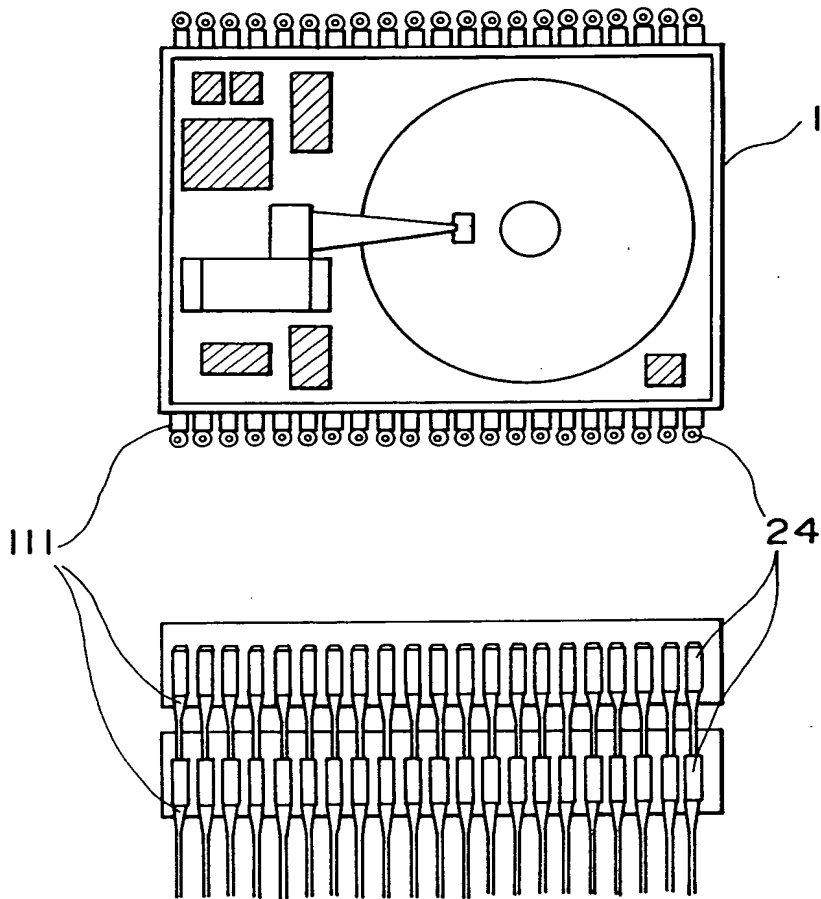
FIG. 14



0001368 0001368

APPROVED	C. C. FIG	
BY	CLASS	RECLASS
DRAFTSMAN		

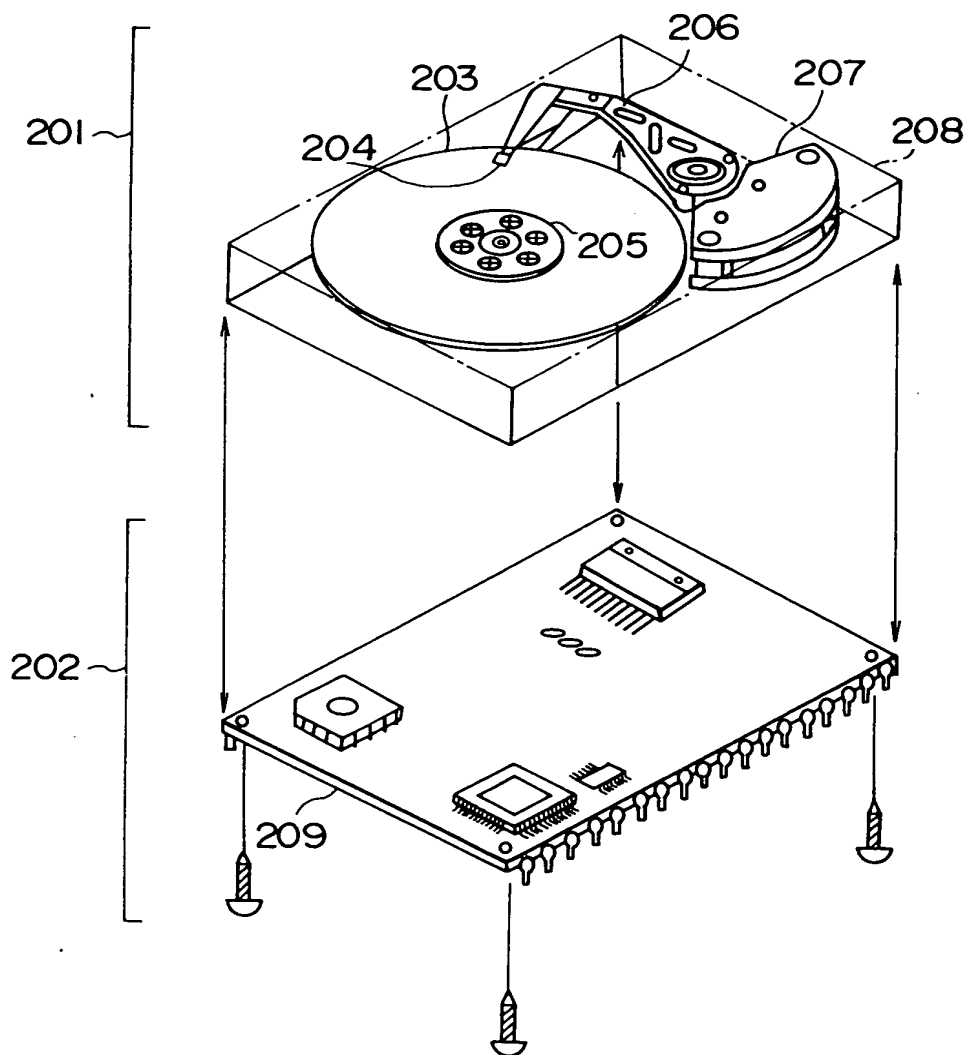
FIG. 17



TOP SECRET

APPROVER	C. C. FIG.	
RV	CLASS	REIRCLASE
DRAFTSMAN		

FIG. 18

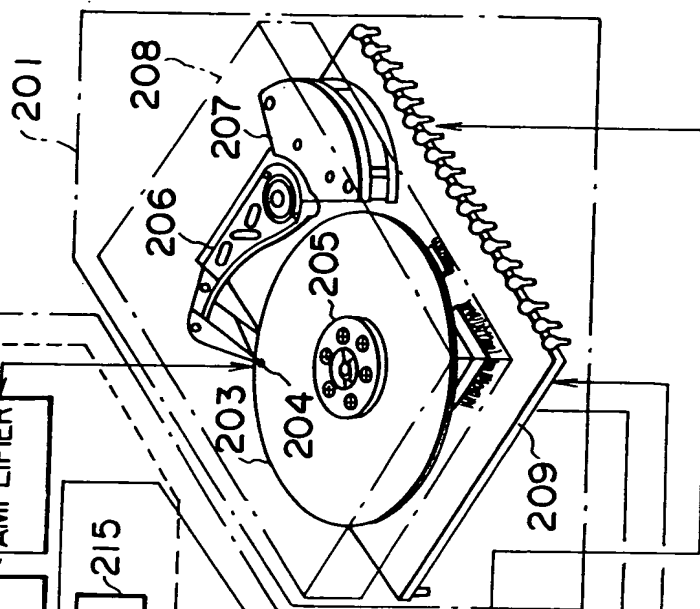


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The diagram illustrates the system architecture of a hard disk drive. An **EXTERNAL HOST** is connected to the drive via a bidirectional interface **212**. The drive's internal components are organized into several functional blocks:

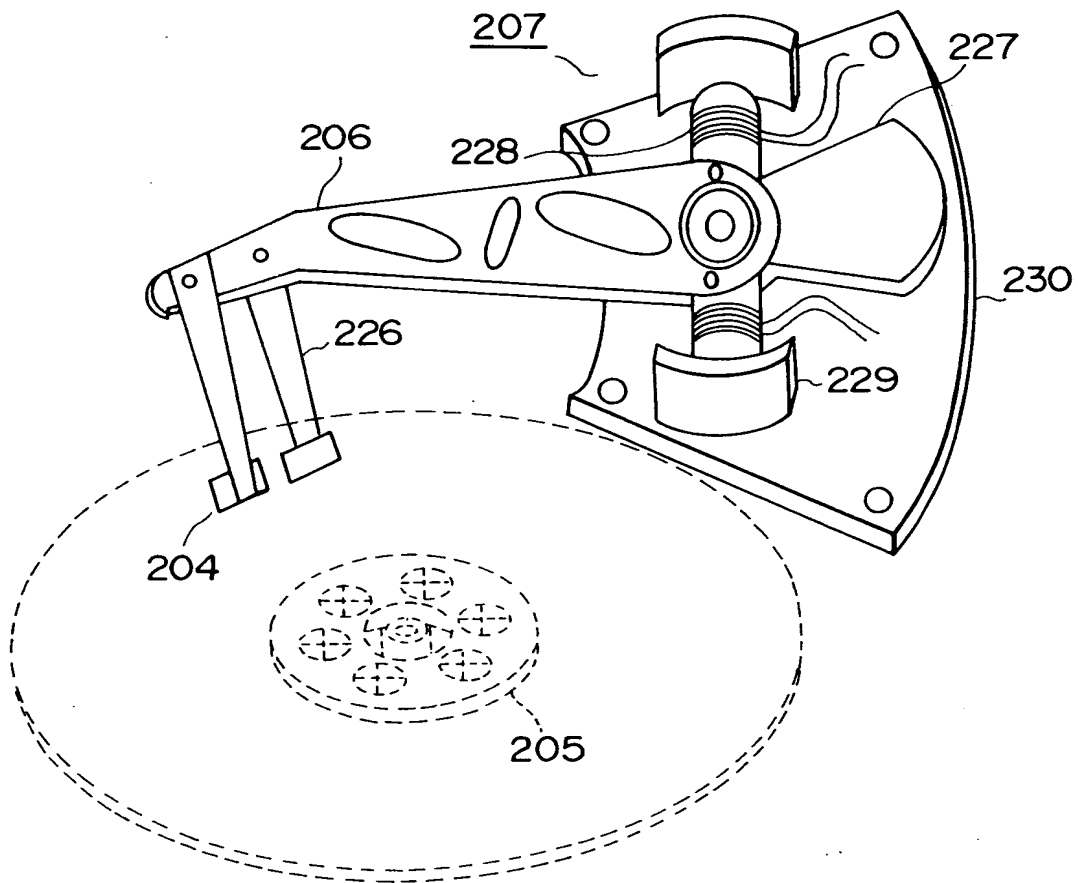
- Host Interface and Control (222):** Includes the **SCSI CONTROLLER** and **BUFFER RAM**, which manage data flow between the host and the drive.
- Central Processing (225):** The **CPU** is connected to the SCSI controller and the **HDC** (Hard Disk Controller).
- Signal Processing (210):** This section contains the **WRITE CLOCK GENERATING CIRCUIT (221)**, **HEAD POSITIONING CONTROL CIRCUIT (218)**, **POSITIONAL SIGNAL GENERATING CIRCUIT (217)**, **MOTOR DRIVER (219)**, and **SPINDLE MOTOR CONTROL/DRIVER (220)**. These circuits manage the timing and positioning of the drive's mechanical components.
- Data Path (214):** Consists of the **WAVEFORM SHAPING CIRCUIT (EQUALIZER)** and **R/W AMPLIFIER**, which prepare signals for the read/write head.
- Data Management (216):** Includes the **FN CODE / CIRCUIT** and **DATA SEPARATOR**, which handle error correction and data formatting.
- Physical Drive Assembly (201):** A detailed view of the disk assembly showing the **DISK (204)**, **READ/WRITE HEAD (205)**, **SPINDLE MOTOR (206)**, and various mechanical components like the **SLIP RING (207)** and **ACTUATOR (208)**.

Interconnections are shown with solid lines for primary data and control paths, and dashed lines for secondary or control signals. The overall system is designed for reliable data storage and retrieval.



APPROVER	C. J. FIG.	
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FIG. 21



TOP SECRET

APPROVED	C.C. FIG.	
BY	CLASS	SUBCLASS
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FIG. 22

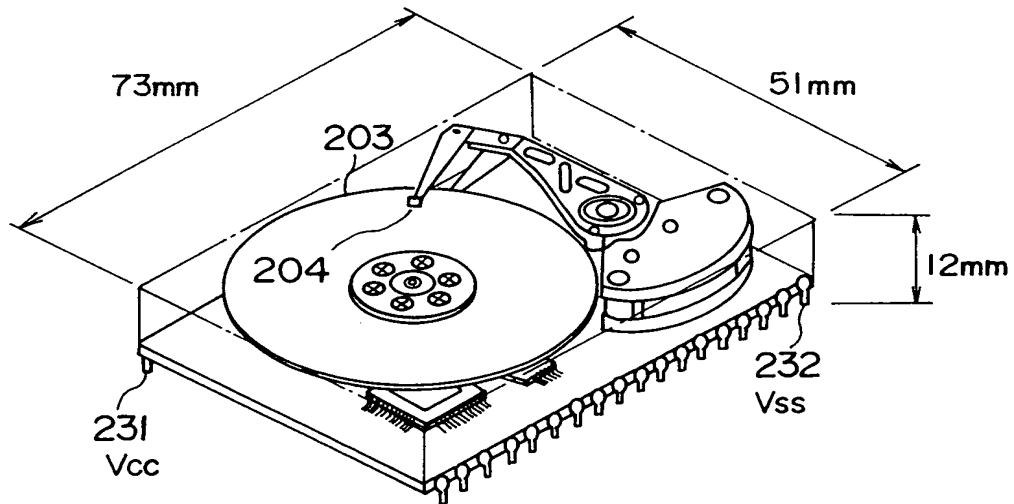


FIG. 22

APPROVER	C. C. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FIG. 23

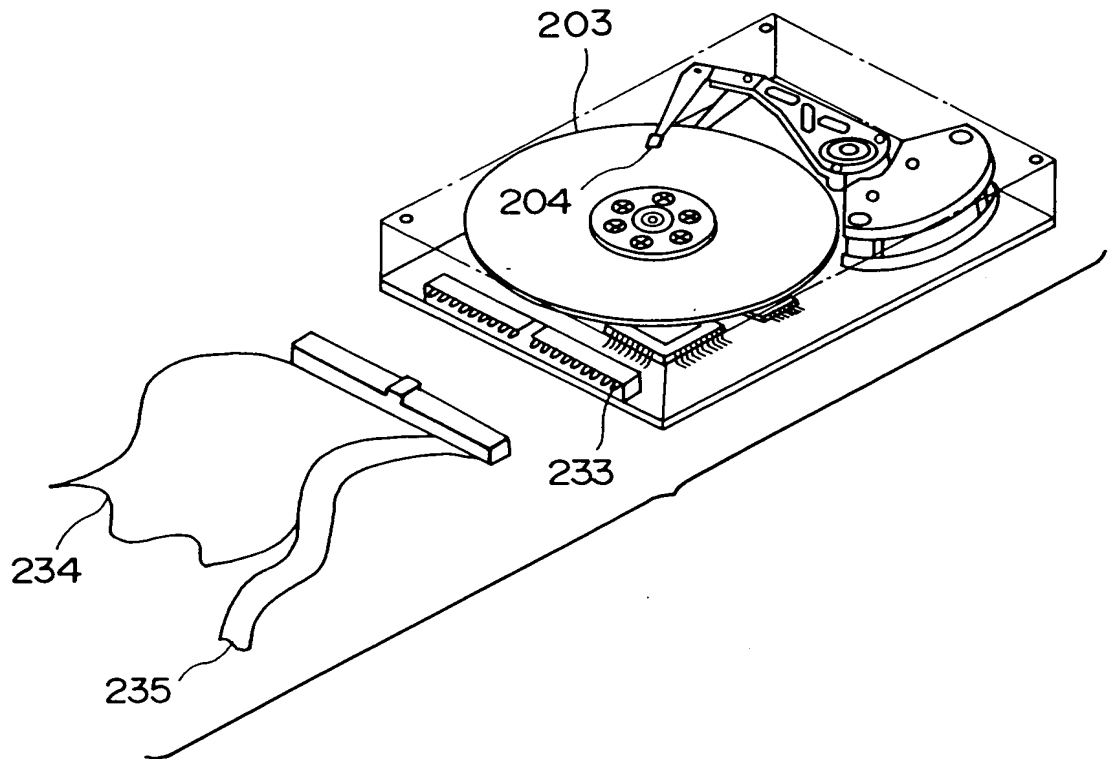
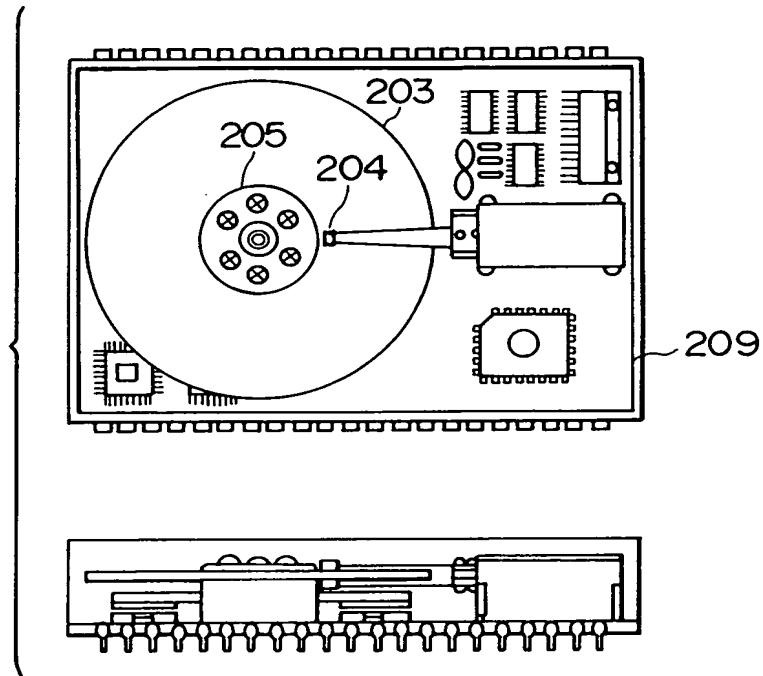


FIG. 23

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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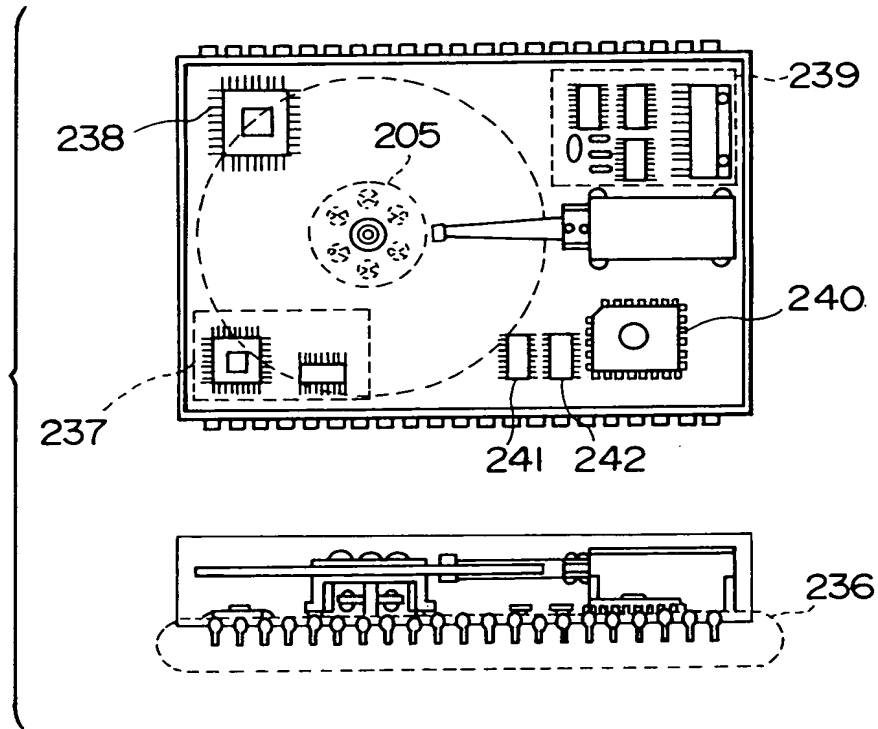
FIG. 24



TOP SECRET

APPROVER	C. S. FIG.	
BY	DATE	REVISION
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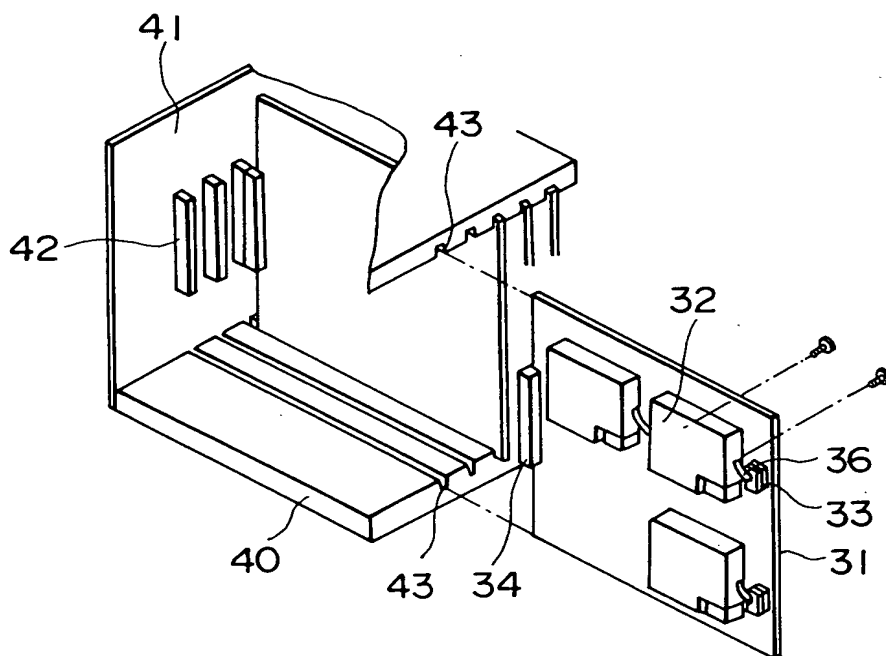
FIG. 25



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APPROVER	O. C. FIG.	
BY	CLASS	SUBCLASS
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FIG. 26
PRIOR ART



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FOI/EO 13526/2001